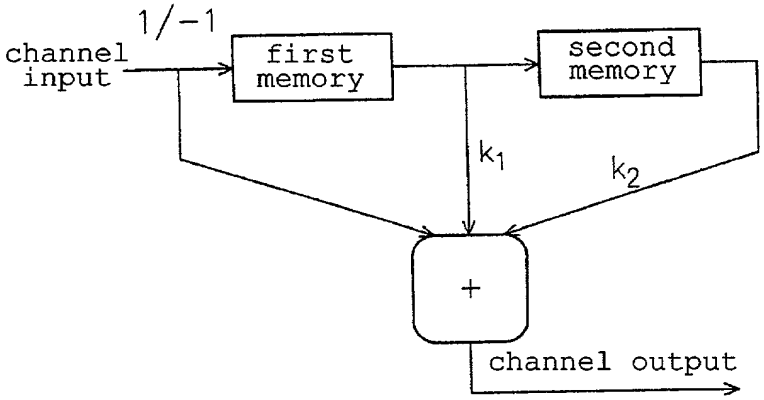


FIG. 1A (Prior Art)

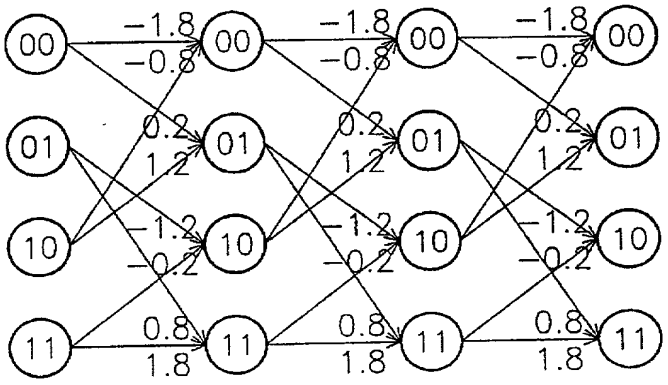


FIG. 1B (Prior Art)

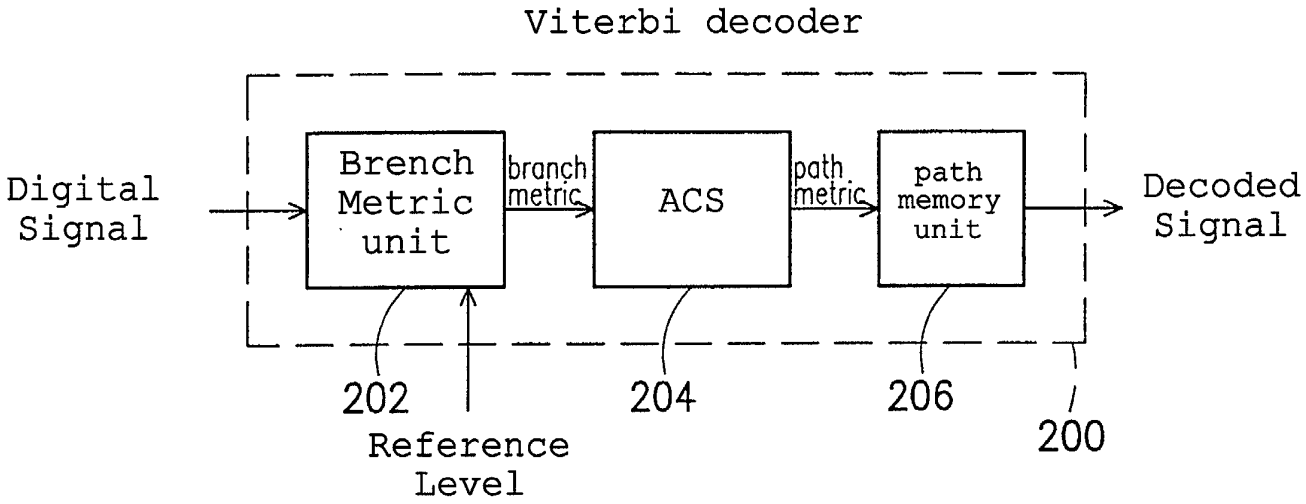
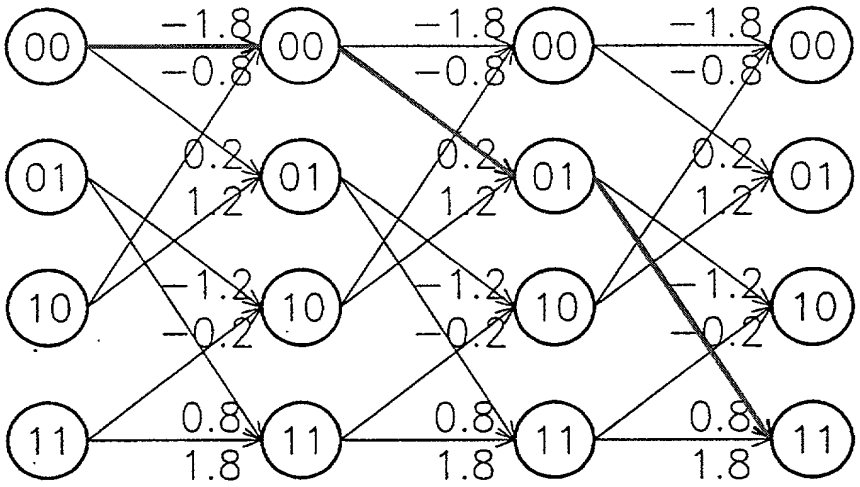


FIG. 2 (Prior Art)



received signal R1	received signal R2	received signal R3	
at 1T	at 2T	at 3T	at 4T

FIG. 3 (Prior Art)

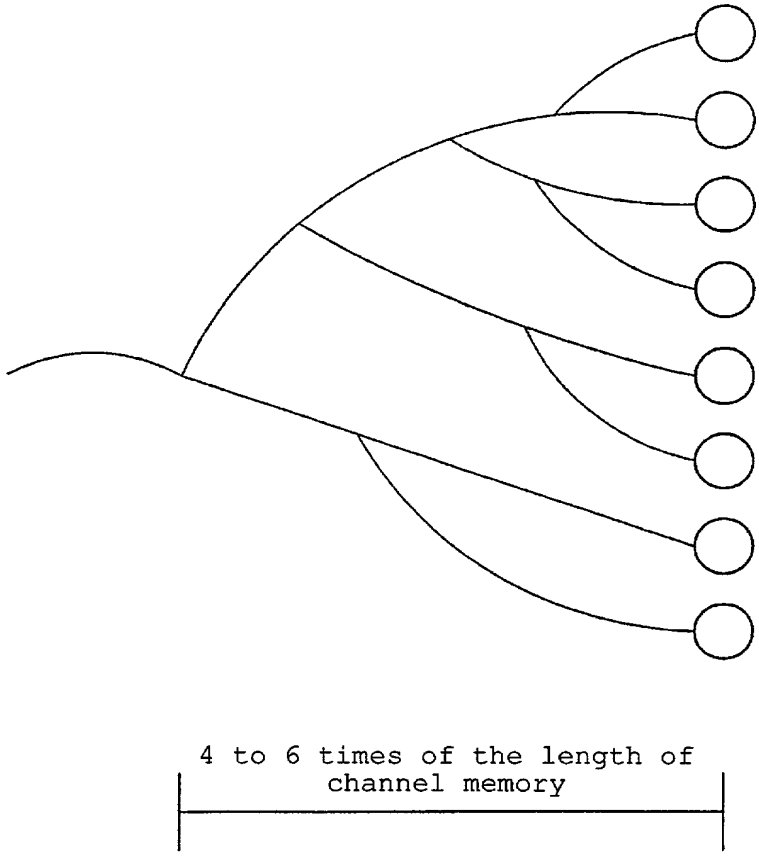


FIG. 4 (Prior Art)

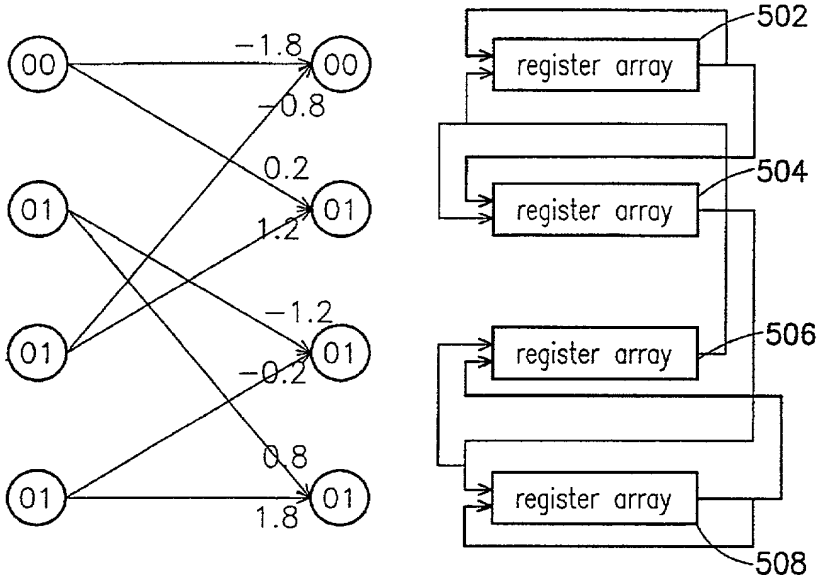


FIG. 5 (Prior Art)

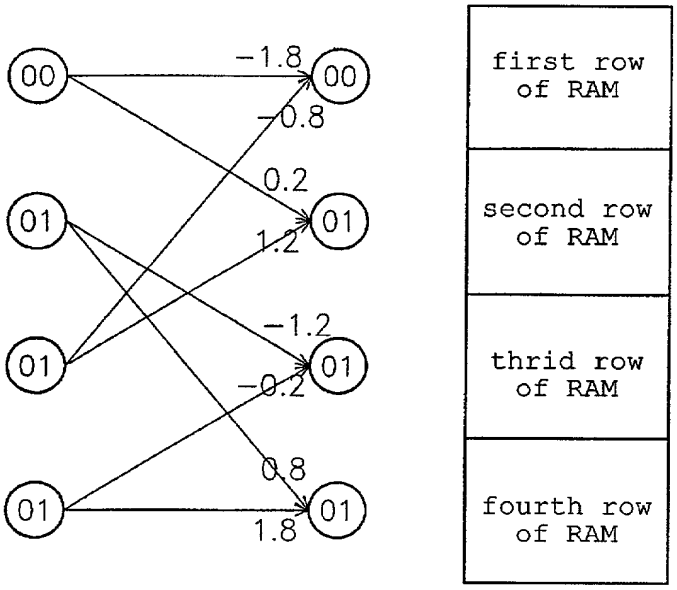


FIG. 6 (Prior Art)

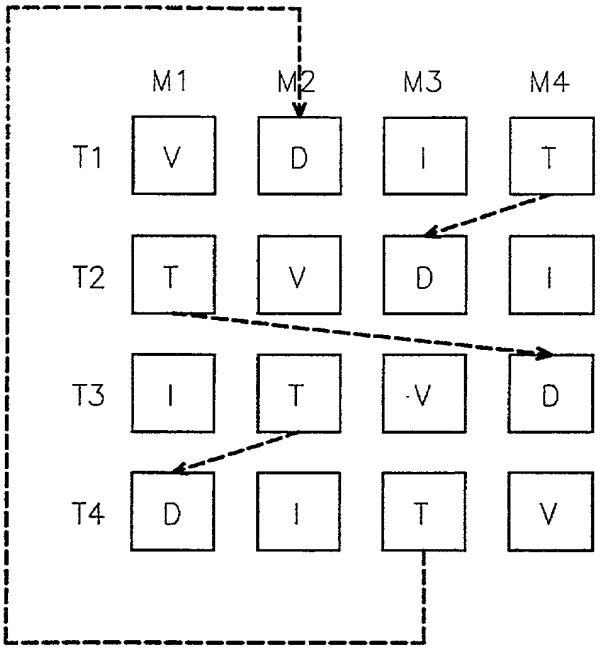


FIG. 7 (Prior Art)

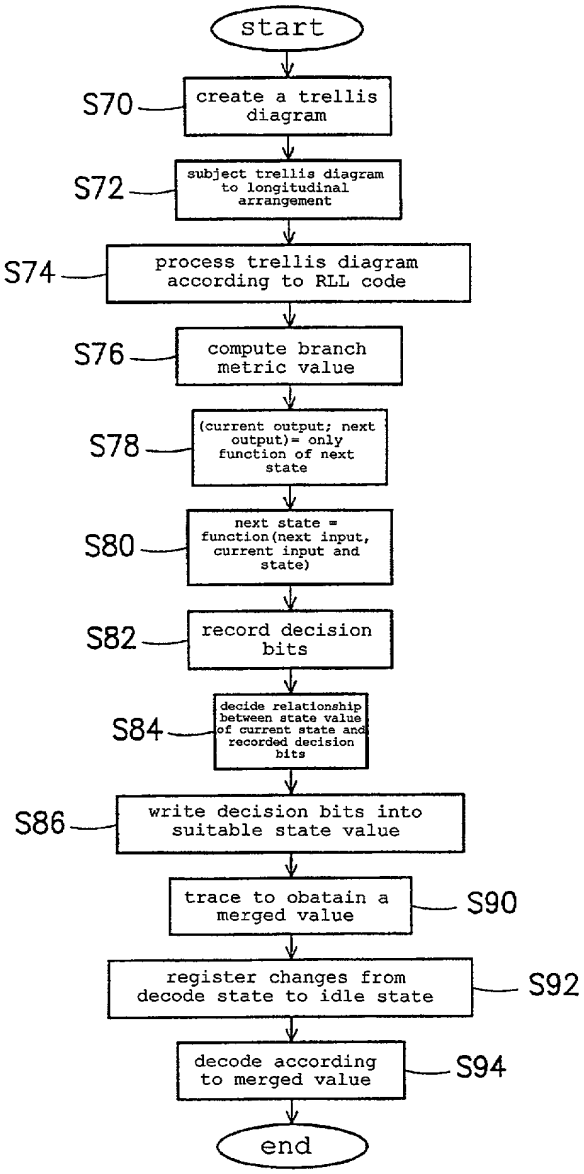

start
S70
create a trellis diagram
S72
subject trellis diagram to longitudinal arrangement
S74
process trellis diagram according to RLL code
S76
compute branch metric value
S78
(current output; next output)= only function of next state
S80
next state = function(next input, current input and state)
S82
record decision bits
S84
decide relationship between state value of current state and recorded decision bits
S86
write decision bits into suitable state value
trace to obatain a merged value
S90
register changes from decode state to idle state
S92
decode according to merged value
S94
end

FIG. 8

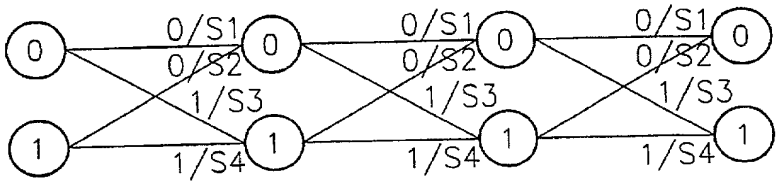


FIG. 9A

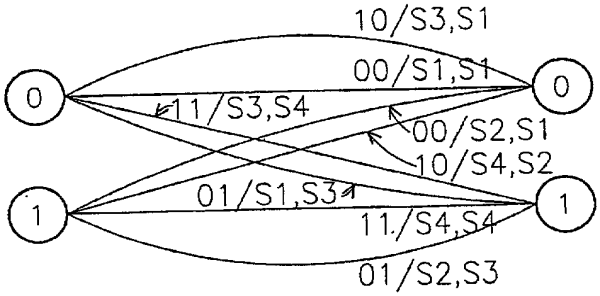


FIG. 9B

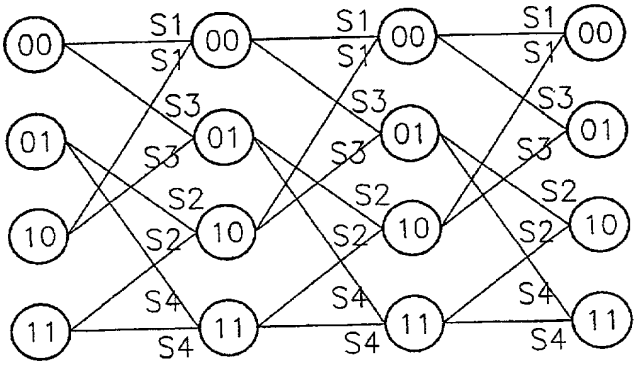


FIG. 9C

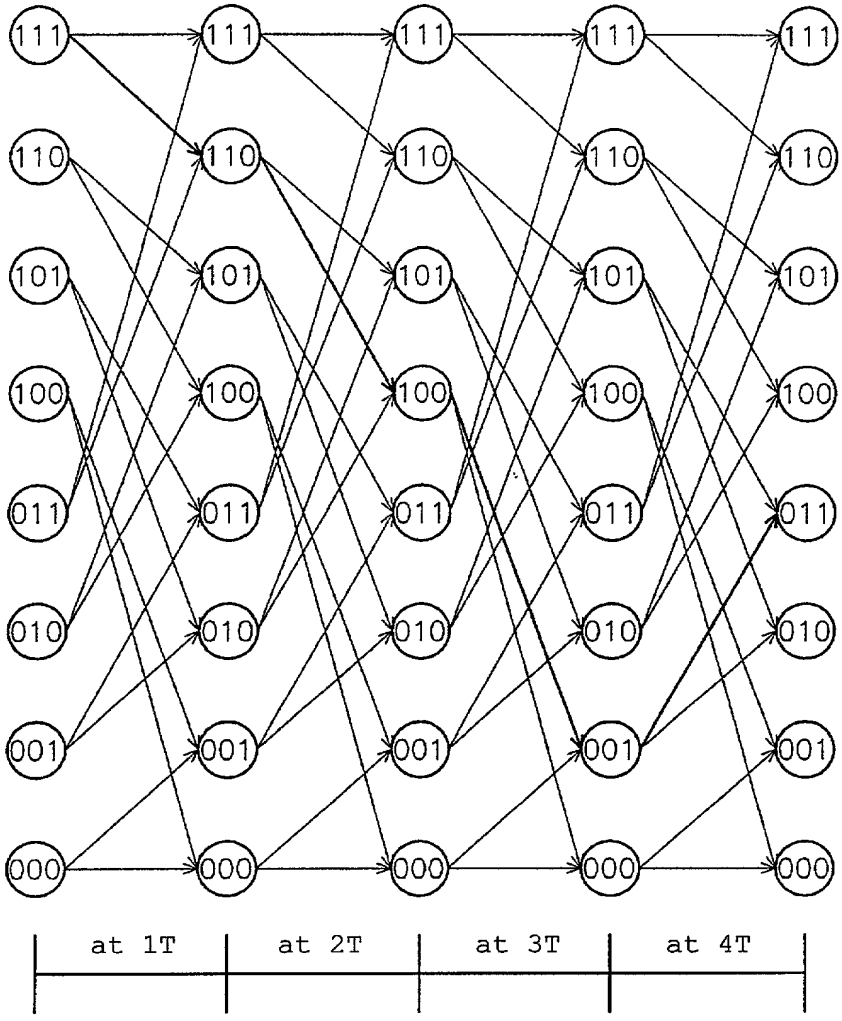


FIG. 10

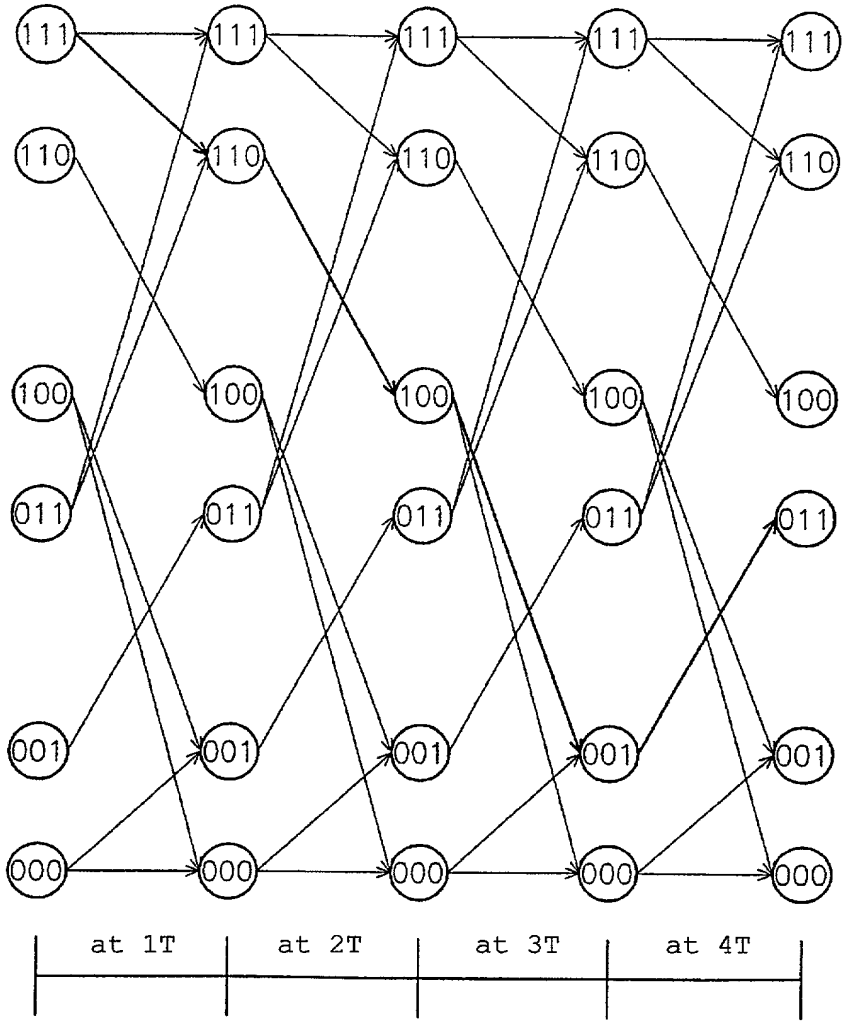


FIG. 11

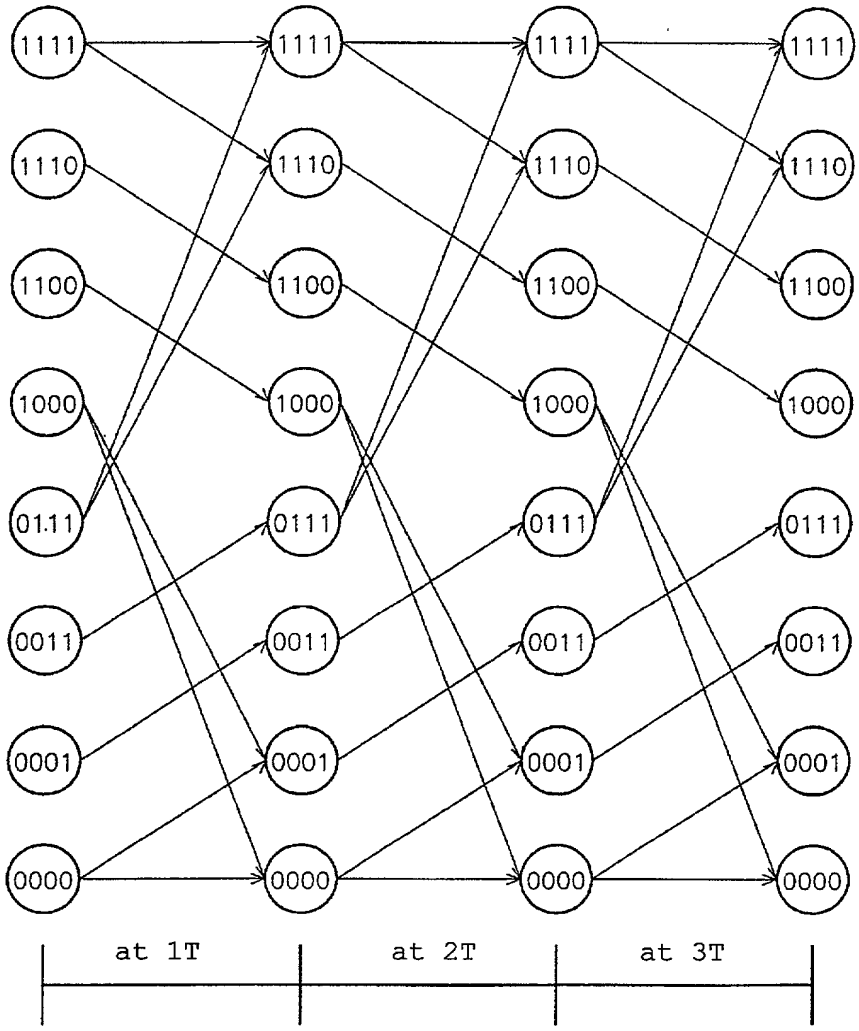


FIG. 12

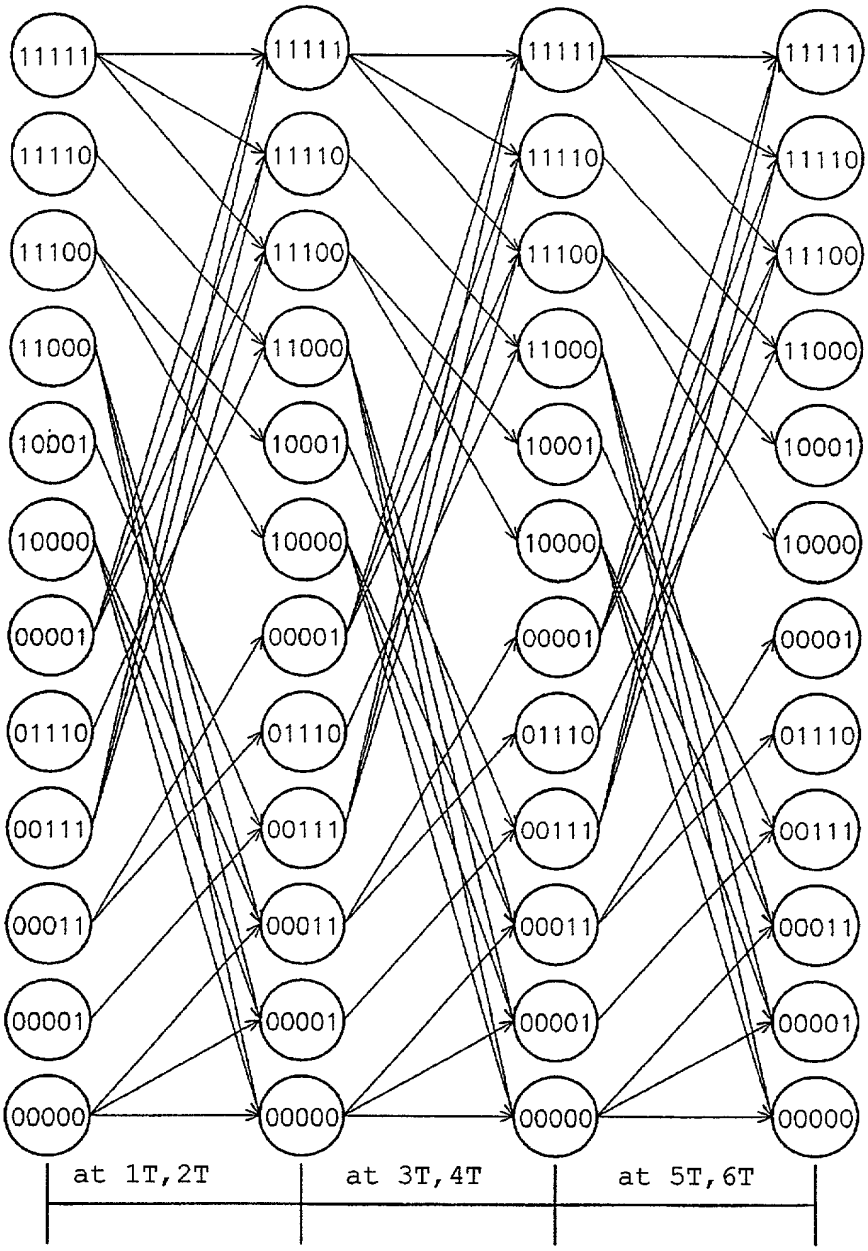

11111
11110
11100
11000
10001
10000
00001
01110
00111
00011
00001
00000
at 1T,2T
at 3T,4T
at 5T,6T

FIG. 13

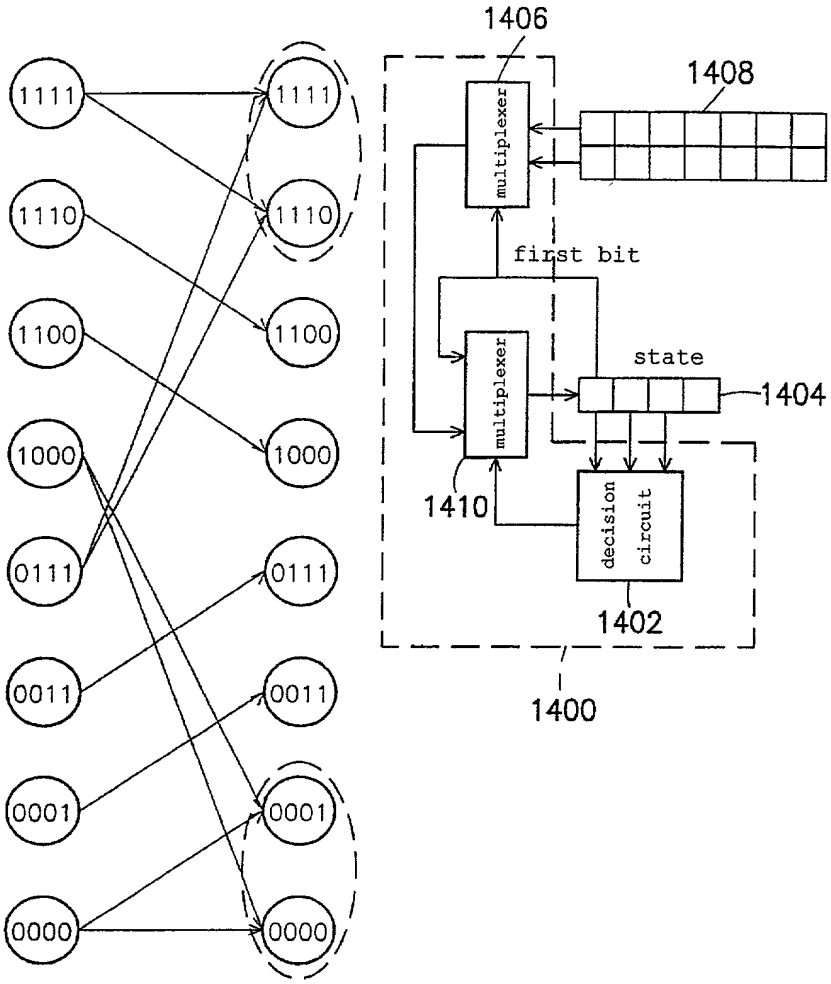

1406
1408
1111
1110
1100
1000
0111
0011
0001
0000
multiplexer
first bit
multiplexer
state
1404
1410
decision circuit
1402
1400

FIG. 14

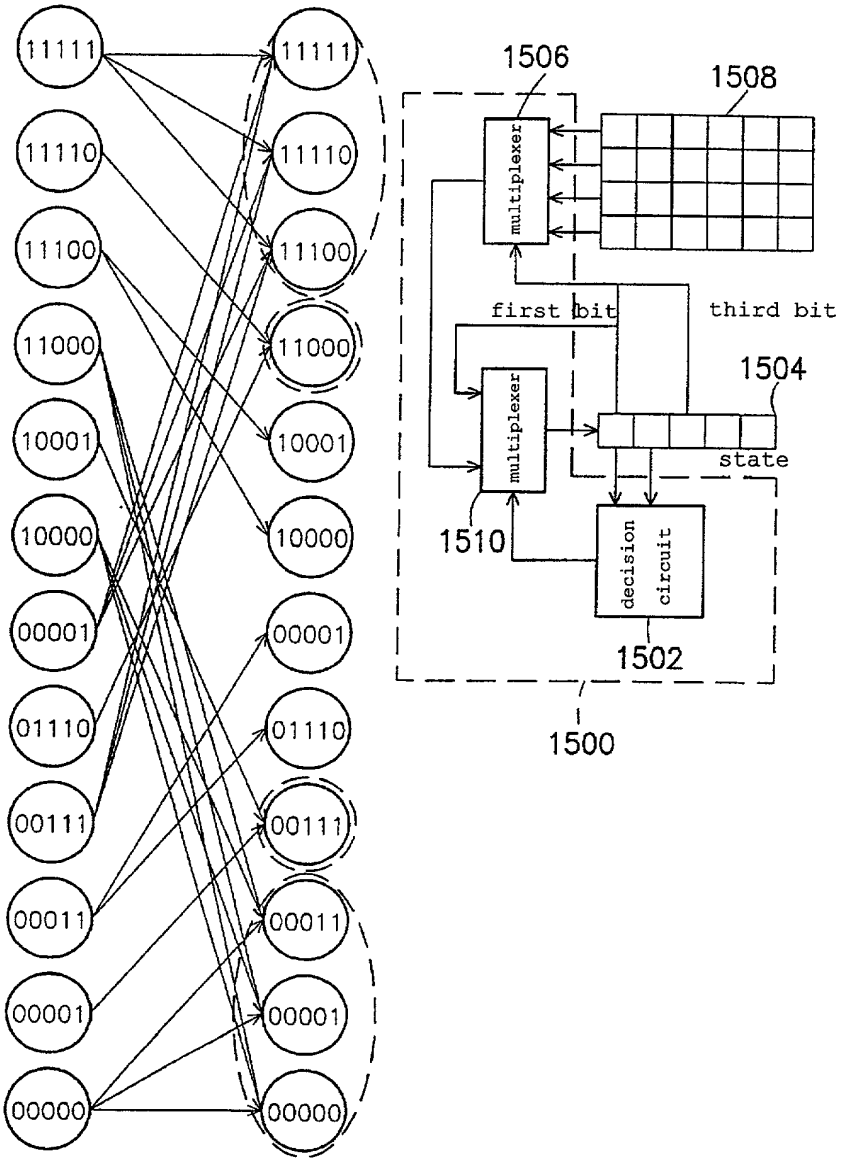

11111
11110
11100
11000
10001
10000
00001
01110
00111
00011
00001
00000
11111
11110
11100
11000
10001
10000
00001
01110
00111
00011
00001
00000
1506
1508
multiplexer
first bit
third bit
1504
multiplexer
state
1510
decision circuit
1502
1500

FIG. 15

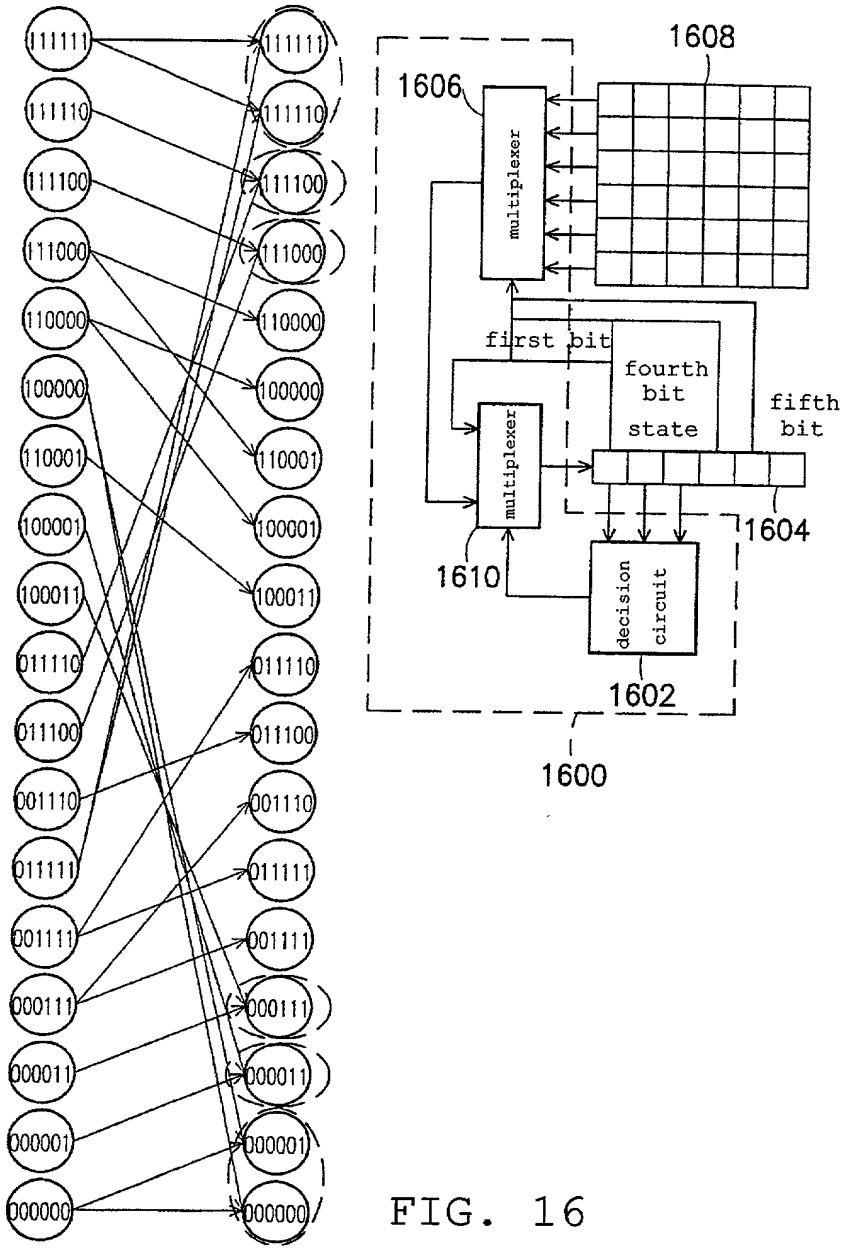

111111
111110
111100
111000
110000
100000
110001
100001
100011
011110
011100
001110
011111
001111
000111
000011
000001
000000
1608
1606
multiplexer
first bit
fourth bit
state
fifth bit
multiplexer
1604
1610
decision circuit
1602
1600

FIG. 16

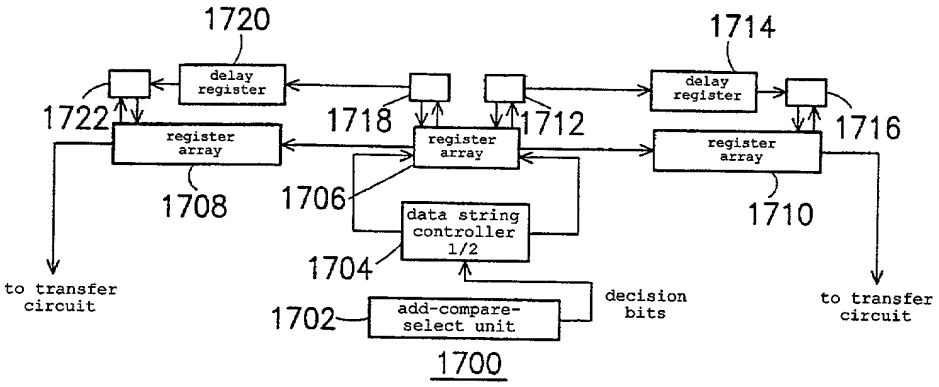


FIG. 17A

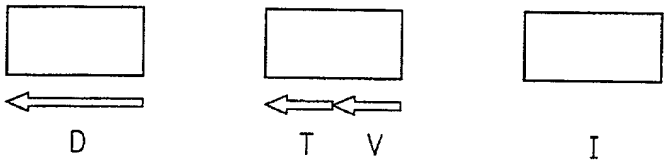


FIG. 17B

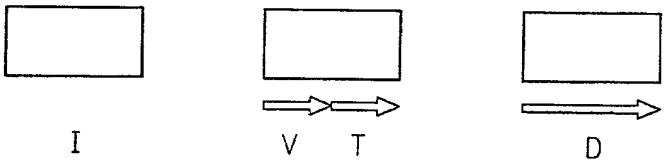


FIG. 17C

decision bits for decoding	dummy data delay	decision bits for decoding	dummy data delay	decision bits for decoding	dummy data delay

FIG. 17D